

UCD30xx

Miscellaneous Analog Control (MAC)

Programmer's Guide

Literature Number: xxxxxx

Date

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1 Miscellaneous Analog Control Summary

The Miscellaneous Analog Control Registers are a catch-all of registers that control and monitor a wide variety of functions.

These registers and peripherals are all available in the UCD3040 80 pin version. Other UCD30xx devices may have reduced resources. Consult the applicable datasheet for details.

1.1 Analog Comparators

There are 3 registers associated with the Analog comparators:

Comparator Control Register (COMPCTRL)
Comparator Read Register (COMPREAD)
CLF Control Register (CLFCTRL)

They are all relatively simple and straightforward, and the reader is referred to the reference section of this document for the descriptions. (Section 2 Miscellaneous Analog Control Reference)

CLFCTRL connects the Comparator outputs to the CLF logic in the DPWM peripherals. For more information on the CLF logic, consult the UCD3000 Fusion Power Peripherals Programmer's Manual.

On the UCD30xx, comparators A through D (sometimes called 1 through 4) share pins with ADC inputs 2 through 5.

Pin Name	Comparator
AD-02/COMP1	COMP_A
AD-03/COMP2	COMP_B
AD-04/COMP3	COMP_C
AD-05/COMP4	COMP_D

1.1.1 COMP_DIS Bit Function

The COMP_DIS bit in the COMPCTRL register not only enables the comparators, it powers them down to save a small amount of power. Therefore it is necessary to clear the COMP_DIS bit before enabling CLF functions or interrupts driven by the comparators. It is possible to get a glitch on the comparator outputs as they are powered up.

1.2 Package ID information

Refer to Section 2.4 Package ID Register (PKGID).

1.3 DPWM synchronization

The SYNCCTRL register is one of several registers – in three different areas of the memory map – that control both the synchronization of the DPWM channels with external events, and the use of the SYNC_IN and

SYNC_OUT pins as general purpose I/O. For a complete discussion, please refer to the UCD3000 Fusion Power Peripherals Programmer's Manual

1.4 JTAG pin use for I/O and JTAG security.

On the lower pin count devices, such as the UCD3020, the IOMUXCTRL register works as described in the reference section below.

On the 80 pin UC2.7D3040, its default initialization value is 0, rather than 1. But if the firmware sets it to a 1, it will disable the JTAG functionality. It will not enable the other outputs. This will prevent anyone from connecting up a JTAG adapter and reading the flash.

The same thing can be accomplished on the smaller pin count devices in the same way, even if it is not desired to use the JTAG pins as I/O.

If reprogramming the flash, or using the JTAG is desired, some method, possibly a special PMBus command, should be provided to unlock the system.

1.5 Brownout

The Brownout Register is also adequately described in the Reference area below (2.7 Brownout Register (BROWNOUT)). For specific thresholds, consult the datasheet.

1.6 CLKCTRL Register – High Frequency Oscillator Filter

The CLKCTRL register is primarily intended for factory use. There are 5 bits in the register. The lower 4 bits should not be changed in any way. Changing these bits will stop the device from operating properly.

The 5th bit is normally reset. Setting this bit may reduce clock jitter, especially in noisy environments.

To set this bit, use the following C language statement:

```
MacRegs.CLKCTRL.bit.HI_OSC_FLT_ENA = 1;
```

The register is described in the reference section below.

2 Miscellaneous Analog Control Reference

2.1 Comparator Control Register (COMPCTRL)

Address FFF7F000

Bit Number	25	24	23:18
Bit Name	COMP_INT_ENA	COMP_DIS	COMP_ADJ_D
Access	R/W	R/W	R/W
Default	0	1	000000

Bit Number	17:12	11:6	5:0
Bit Name	COMP_ADJ_C	COMP_ADJ_B	COMP_ADJ_A
Access	R/W	R/W	R/W
Default	000000	000000	000000

Bit 25: COMP_INT_ENA – Analog Comparators Interrupt Enable

0 = Disables Analog Comparator Interrupt (Default)

1 = Enables Analog Comparator Interrupt

Bit 24: COMP_DIS – Analog Comparators Disable

0 = Enables Analog Comparators

1 = Disables Analog Comparators (Default)

Bits 23-18: COMP_ADJ_D – Reference Select for Analog Comparator D

000000 = Comparator Reference of 31.250 mV (Default)

000001 = Comparator Reference of 62.5 mV

.....

111111 = Comparator Reference of 2.0 V

Bits 17-12: COMP_ADJ_C – Reference Select for Analog Comparator C

000000 = Comparator Reference of 31.250 mV (Default)

000001 = Comparator Reference of 62.5 mV

.....

111111 = Comparator Reference of 2.0 V

Bits 11-6: COMP_ADJ_B – Reference Select for Analog Comparator B

000000 = Comparator Reference of 31.250 mV (Default)

000001 = Comparator Reference of 62.5 mV

.....

111111 = Comparator Reference of 2.0 V

Bits 5-0: COMP_ADJ_A – Reference Select for Analog Comparator A

000000 = Comparator Reference of 31.250 mV (Default)

000001 = Comparator Reference of 62.5 mV

.....

111111 = Comparator Reference of 2.0 V

2.2 Clock Control Register (CLKCTRL)

Address FFF7F004

Bit Number	4	3	2:1	0
Bit Name	HI_OSC_FLT_ENA	LO_OSC_DIS	HI_OSC_TRIM	HI_OSC_ENA
Access	R/W	R/W	R/W	R/W
Default	0	0	XX	1

WARNING – Do not change bits 0 to 3. Changing bits 0 to 3 may cause the device to cease operation. They will cause the device to not meet its specification.

Bit 4: HI_OSC_FLT_ENA - High Frequency Oscillator Low Noise Filter Enable – this bit can be changed

0 = Disables 30KHz Low Noise Filter (Default)

1 = Enables 30KHz Low Noise Filter

Bit 3: LO_OSC_DIS - Low Frequency Oscillator Disable – do not change this bit

0 = Enables Low Frequency Oscillator Clock (Default)

1 = Disables Low Frequency Oscillator Clock

Bits 2-1: HI_OSC_TRIM - High Frequency Oscillator Thermal Coefficient Trim – do not change these bits

00 = Trim value 0 (Default)

01 = Trim value 1

10 = Trim value 2

11 = Trim value 3

Bit 0: HI_OSC_ENA - High Frequency Oscillator Enable – do not change this bit.

0 = Disables High Frequency Oscillator

1 = Enables High Frequency Oscillator (Default)

2.3 Comparator Read Register (COMPREAD)

Address FFF7F01C

Bit Number	4	3	2	1	0
Bit Name	COMP_INT	COMP_D	COMP_C	COMP_B	COMP_A
Access	R	R	R	R	R
Default	-	-	-	-	-

Bit 4: COMP_INT – Analog Comparator Interrupt

0 = Analog Comparator Interrupt is not asserted

1 = Analog Comparator Interrupt is asserted

Bit 3: COMP_D - Comparator D Status

0 = Analog Comparator D is unset

1 = Analog Comparator D has been set (Tripped)

Bit 2: COMP_C - Comparator C Status

0 = Analog Comparator C is unset

1 = Analog Comparator C has been set (Tripped)

Bit 1: COMP_B - Comparator B Status

0 = Analog Comparator B is unset

1 = Analog Comparator B has been set (Tripped)

Bit 0: COMP_A - Comparator A Status

0 = Analog Comparator A is unset

1 = Analog Comparator A has been set (Tripped)

2.4 Package ID Register (PKGID)

Address FFF7F020

Bit Number	1:0
Bit Name	PKG_ID
Access	R
Default	-

Bits1-0: PKG_ID – Represents package type of device

00 = 80-pin package

01 = 64-pin package

10 = 48-pin package

11 = reserved for future use

2.5 Sync Control Register (SYNCCTRL)

Address FFF7F024

Bit Number	17	16	15:6	5:4
Bit Name	SYNC_OUT_IN	SYNC_INPUT_IN	RESERVED	SYNC_MUX_SEL
Access	R	R	-	R/W
Default	-	-	0000_0000_00	00

Bit Number	3	2	1	0
Bit Name	RESERVED	SYNC_OUTPUT_DIR	SYNC_INPUT_OUT	SYNC_INPUT_DIR
Access	-	R/W	R/W	R/W
Default	0	1	1	1

Bit 17: SYNC_OUT_IN – Value of SYNC_OUTPUT pin when configured as GPIO

0 = Logic level low present on SYNC_OUTPUT pin

1 = Logic level high present on SYNC_OUTPUT pin

Bit 16: SYNC_INPUT_IN – Value of SYNC_INPUT pin when configured as GPIO

0 = Logic level low present on SYNC_INPUT pin

1 = Logic level high present on SYNC_INPUT pin

Bit 15-6: RESERVED – Unused bits in current application

Bits 5-4: SYNC_MUX_SEL – Selects which loop controls SYNC_OUTPUT

00 = Loop 1 Sync Output (Default)

01 = Loop 2 Sync Output

10 = Loop 3 Sync Output

11 = Loop 4 Sync Output

Bit 3: RESERVED – Unused bits in current application

Bit 2: SYNC_OUTPUT_DIR – Configures direction of SYNC_OUTPUT pin

0 = SYNC_OUTPUT pin configured as an output pin

1 = SYNC_OUTPUT pin configured as an input pin (Default)

Bit 1: SYNC_INPUT_OUT – Configure output value for SYNC_INPUT pin, if used as an output

0 = SYNC_INPUT pin driven low in output mode

1 = SYNC_INPUT pin driven high in output mode (Default)

Bit 0: SYNC_INPUT_DIR – Configure direction of SYNC_INPUT pin

0 = SYNC_INPUT pin configured as an output pin

1 = SYNC_INPUT pin configured as an input pin (Default)

2.6 I/O Functional Multiplexer Control Register (IOMUXCTRL)

Address FFF7F028

Bit Number	2:0
Bit Name	IO_FUNC_MODE
Access	R/W
Default	000 or 001

Bits 2-0: IO_FUNC_MODE - Provides multiplexing pin options for the JTAG pins in smaller pin package devices

000/111 = JTAG mode (000 is default for UCD3040 80 pin device)

001 = GPIO/SPI mode (Default for reduced pin count devices)

010 = SCI, Sync In, Clock Out

011 = Faults, Clock Out, Sync In

100 = SCI, External Interrupts

101 = Clock Out, Sync In, External Interrupts

Bits								
Pin Name	Pin # (64/48/32)	"111" "110" "000"	"001"	"010"	"011"	"100"	"101"	"110"
TMS	39/31/20	TMS	SPI-CS/ GPIO-38	SYNC- OUT	FAULT- 2B	INT1	INT1	INT1
TDI	38/30/19	TDI	SPI-DI/ GPIO-39	SCI-RX	FAULT- 1B	SCI-RX	SYNC-IN	TCAP0
TDO	37/29/18	TDO	SPI-DO/ GPIO-40	SCI-TX	SYNC- OUT	SCI-TX	SYNC- OUT	TCOMPARE
TCK	36/28/17	TCK	SPI-CLK/ GPIO-41	SYNC-IN	SYNC-IN	INT2	INT2	TCAP1

2.7 Brownout Register (BROWNOUT)

Address FFF7F02C

Bit Number	2	1	0
Bit Name	INT	INT_EN	COMP_EN
Access	R	R/W	R/W
Default	-	0	0

Bit 2: INT – Brownout Interrupt Status

0 = No Brownout Condition observed

1 = Brownout Condition observed

Bit 1: INT_EN – Brownout Interrupt Enable

0 = Brownout Interrupt disabled (Default)

1 = Brownout Interrupt enabled

Bit 0: COMP_EN – Brownout Comparator Enable

0 = Brownout comparator logic disabled (Default)

1 = Brownout comparator logic enabled

2.8 CLF Control Register (CLFCTRL)

Address FFF7F030

Bit Number	7:6	5:4	3:2	1:0
Bit Name	L4_CLF_CTRL	L3_CLF_CTRL	L2_CLF_CTRL	L1_CLF_CTRL
Access	R/W	R/W	R/W	R/W
Default	11	10	01	00

Bits 7-6: L4_CLF_CTRL – Selects connection for Loop 4 CLF Input

- 00 = Routed from output of Analog Comparator A
- 01 = Routed from output of Analog Comparator B
- 10 = Routed from output of Analog Comparator C
- 11 = Routed from output of Analog Comparator D (Default)

Bits 5-4: L3_CLF_CTRL – Selects connection for Loop 3 CLF Input

- 00 = Routed from output of Analog Comparator A
- 01 = Routed from output of Analog Comparator B
- 10 = Routed from output of Analog Comparator C (Default)
- 11 = Routed from output of Analog Comparator D

Bits 3-2: L2_CLF_CTRL – Selects connection for Loop 2 CLF Input

- 00 = Routed from output of Analog Comparator A
- 01 = Routed from output of Analog Comparator B (Default)
- 10 = Routed from output of Analog Comparator C
- 11 = Routed from output of Analog Comparator D

Bits 1-0: L1_CLF_CTRL – Selects connection for Loop 1 CLF Input

- 00 = Routed from output of Analog Comparator A (Default)
- 01 = Routed from output of Analog Comparator B
- 10 = Routed from output of Analog Comparator C
- 11 = Routed from output of Analog Comparator D

Vdd